

The AMBA Bus Architecture and Protocols

Summary:

This course forms a comprehensive introduction to the popular AMBA AXI4 on-chip interconnect protocol. It describes the main features of the protocol, together with a number of typical use cases.

Prerequisites:

- A working knowledge of system-on-chip design

Audience:

The course is aimed at Hardware and Software Engineers needing to get an overview of the features, capability and application of the AMBA AXI4 protocol.

Delivery Method:

- Online

Length:

- 1 hour

Modules:

1. AMBA evolution and AXI protocol overview

- What is AMBA and why use it?
- How has AMBA evolved?
- The AXI protocol
- The AXI protocol in multi-master system design
- AXI channels

2. Channel transfers and transactions

- Main AXI features
- Channel handshake
- The difference between transfers and transactions
- Examples of channel transfers
- Write transaction behavior - single data item
- Write transaction behavior - multiple data items
- Read transaction behavior - single data item
- Read transaction behavior - multiple data items
- Active transactions

3. Channel signals in detail

- Data size, length, and burst type
- Protection level support
- Cache support
- Response signalling
- Write data strobes
- Atomic accesses with the lock signal
- Quality of service
- Region signalling and user signals
- AXI channel dependencies
- Read channel signals
- Write channel signals

4. Atomic accesses

- Two types of atomic access
- Locked access overview
- Locked access operation
- Exclusive access overview
- Exclusive access hardware monitor operation
- Exclusive transaction pairs - pass/pass
- Exclusive transaction pairs - pass/fail

5. Transfer behavior and transaction ordering

- Examples of simple transactions
- Transfer IDs
- Write transaction ordering rules
- Read transaction ordering rules
- Read and write channel ordering
- Unaligned transfer start address
- Endianness support
- Write interface attributes
- Read interface attributes